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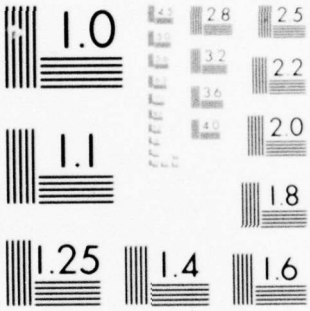

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SOLID PHASE EPITAXIAL GROWTH

C.L. Anderson and J.A. Roth

Hughes Research Laboratories
3011 Malibu Canyon Road
Malibu, CA 90265

October 1977

Contract N00014–75–C–0957
Annual Progress Report
1 May 1976 through 30 April 1977

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Prepared For
OFFICE OF NAVAL RESEARCH
Arlington, VA 22217

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REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

4. TITLE (and Subtitle)

6 SOLID PHASE EPITAXIAL GROWTH

5. TYPE OF REPORT & PERIOD COVERED

9 Annual Progress Report, 1 May [redacted]76-30 Apr[redacted] [redacted]77

6. PERFORMING ORG. REPORT NUMBER

7. AUTHOR(s)

10 J.A. Roth [redacted] C.L. Anderson

8. CONTRACT OR GRANT NUMBER(s)

15 N00014-75-C-0957

9. PERFORMING ORGANIZATION NAME AND ADDRESS

Hughes Research Laboratories
3011 Malibu Canyon Road
Malibu, California 90265

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS

11 Oct 77

11. CONTROLLING OFFICE NAME AND ADDRESS

Office of Naval Research
Department of the Navy
Arlington, VA 22217

12. REPORT DATE

~~November~~ Oct 1977

13. NUMBER OF PAGES

~~50~~ 12 47p.

14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)

15. SECURITY CLASS. (of this report)

Unclassified

15a. DECLASSIFICATION DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

DISTRIBUTION STATEMENT A
Approved for public release;
Distribution Unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Epitaxy
Silicon
Thin films
Crystal growth

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Low-temperature epitaxial growth of Si by the solid-phase epitaxy (SPE) process has been studied to determine the effects of contaminants upon the growth process. The major sources of process-induced contaminants in SPE have been reviewed, and methods for eliminating or minimizing these have been developed. We show that under clean conditions an evaporated (amorphous) Si film will crystallize epitaxially on a Si(100) substrate when heated to 525°C, but that the growth is very sensitive

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to inhibition by atmospheric contaminants. Similarly, SPE growth in the system Si/Pd_2Si/Si(a) has been found to proceed very differently under clean conditions as compared to the standard processing used in previous work. This difference is tentatively attributed to affects of contaminants on the Pd_2Si interlayer, not on the Si(a) film as was previously believed.

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SECTION 1

INTRODUCTION

Solid-phase epitaxy (SPE) is a unique low-temperature process for growing epitaxial, single-crystal semiconductor films. SPE differs from the more familiar epitaxial growth methods, such as vapor-phase epitaxy (VPE) and liquid-phase epitaxy (LPE), in that the source of atoms in the disordered state is a solid amorphous film, and that crystal growth proceeds by totally solid-state processes. For Si, with which we deal exclusively in this report, epitaxial growth by SPE occurs at temperatures in the 400 to 600°C range, about one-half the temperature used in conventional Si epitaxy (e.g., pyrolysis of silane at 1000 to 1200°C).

The simplest type of SPE is done by depositing an amorphous Si film onto a room-temperature single-crystal Si substrate and then heating it to induce epitaxial crystallization of the deposited film. But because this process is extremely sensitive to substrate contaminants, however, nearly all reported examples of SPE growth of Si (Refs. 2 through 5) have used a different process which we will refer to as metal-interlayer SPE. In this process, shown in Figure 1, either a solid solution or compound is formed by reacting a metal interlayer with the adjoining Si layers. This initial step generates a clean substrate for subsequent nucleation and growth of an epitaxial film (as shown in Figure 1 (c and d)).

Although using a metal interlayer in SPE does reduce substrate contamination problems, there is strong evidence that other contaminants introduced during film deposition or subsequent heat treatment can substantially affect the SPE growth process and the physical microstructure of the resulting epitaxial layers. The electrical characteristics of such layers may also depend partially on the introduction of contaminants during the growth process. An obvious example of this would be the incorporation of metal atoms from the metallic interlayer into the grown epitaxial film. More subtle effects related to the generation of crystallographic defects caused by impurity complexes or inclusions are also possible.

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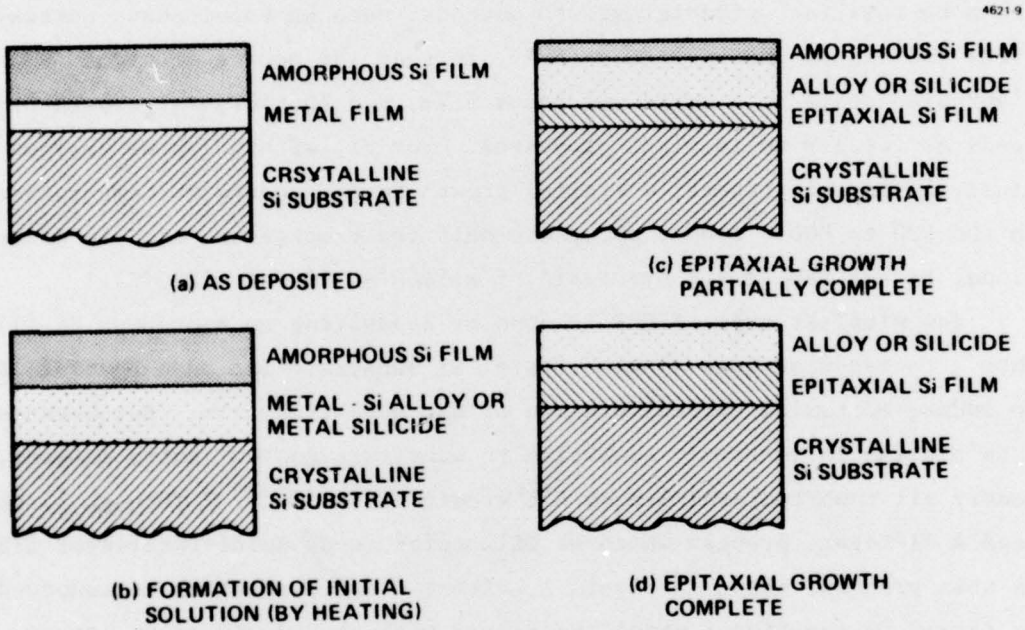

Figure 1. Depiction of solid-phase epitaxy using a metallic interlayer.

Two characteristics of SPE, low temperature and totally solid-phase reactions, will probably cause the sensitivity to contaminants to be higher than in LPE or VPE growth. Therefore, it is important to identify and control process-induced contaminants or their effects if SPE is ever to be useful for growing device-quality epitaxial films. Additionally, there is substantial experimental evidence that the reaction kinetics, physical structure, etc., of SPE films grown by the metal-interlayer approach are seriously affected by contaminants.

We have followed a two-fold approach to studying the effects of process-induced contaminants: (1) establish the capability to grow epitaxial films under non-contaminating conditions and then (2) selectively add impurities or relax the processing conditions until contaminant effects become observable. Nearly all of our efforts have dealt with the first phase of this approach (i.e., the growth of uncontaminated SPE films). The results have been rather dramatic: (1) for the first time, epitaxial Si has been grown by SPE without a metal interlayer, and (2) important differences between metal-interlayer SPE carried out in UHV and all previously reported SPE have been observed.

Intentional impurity introduction has so far been limited to examining the effects of exposure to two grossly contaminating ambients, room air and vacuum furnace ambient (10^{-7} Torr). This exposure dramatically affects metal-free SPE, and experiments are in progress to determine the contaminant effects in detail. In the case of SPE using a Pd_2Si interlayer, however, two different behaviors with respect to contaminants have been observed, depending on the specific details of the processing sequence used. The available data suggest that the microstructure of the Pd_2Si interlayer may play an important role in determining the susceptibility of the SPE growth process to contaminant effects. This area has not previously been explored; but it is possible to rationalize some previously unexplainable results by considering the role of the interlayer in SPE.

We will discuss some of the major sources of contamination in SPE and review the published evidence that contaminant effects are important in determining the outcome of the SPE process. We will then briefly summarize the experimental techniques and apparatus used in studying contaminant effects and present the results of our work. The experimental results will be discussed in terms of a crude model of Si SPE in which contaminants are assumed to be absent. We will also present some preliminary thoughts on the possible mechanisms by which impurity effects could be manifested in SPE, and suggest further experiments to advance our understanding of the SPE growth process.

SECTION 2

SOURCES OF CONTAMINATION IN SPE

At least three major process steps in SPE may introduce contaminants: (1) preparation of the Si substrate, (2) deposition of thin films, and (3) heating to induce growth. Additionally, between each of these steps the sample may be exposed to room air. In this section we briefly review these sources of contamination and indicate, where appropriate, the evidence for contaminant effects in prior work on SPE. We also summarize our approach to eliminating those effects.

Contamination on the substrate Si wafer surface already has been mentioned as the major impediment to achieving SPE by simple amorphous Si deposition followed by heating. Consequently, all reported processes for successful SPE have of necessity incorporated some means of eliminating this internal source of contamination. In all work on Si SPE except our own, a predeposited metal film has been used to disperse the substrate oxide and produce a suitable environment for nucleation and growth. Some of the earliest work involved using simple metals such as Ag, Au, and Al deposited on the substrate before the deposition of amorphous Si. The metal was thought to function as a traveling solvent for Si atoms that had dissolved from the amorphous film and which were supplied to the substrate/metal interface.[2] The nucleation and growth of Si was often sporadic and nonuniform, and this result was attributed to the presence of a thin native oxide on the substrate.[2] Apparently, the reaction between Si and nontransition metals at low temperature is not vigorous enough to break up the native oxide uniformly. One method of overcoming this problem is to use a transition metal interlayer (Pd works well) that reacts during initial heating with the Si on both sides to form a compound (e.g., Pd_2Si).[6] This reaction apparently has the beneficial side effect of dispersing the substrate contaminant layer, thereby providing a "virgin" interface for subsequent epitaxial growth.

Another approach to eliminating substrate contaminants has been successful with Au on Si. The substrate/metal combination is held near the eutectic temperature during Si deposition, which presumably causes the substrate contaminants to go into solution in the metal (or eutectic) film.[5,7]

A variant of the metal-interlayer method was used by Ottaviani et al.[8] to achieve SPE growth in the Ge(x)/Al/Ge(a) system. They employed Ar^+ back-sputtering in a sputter-deposition chamber to partially clean the Ge substrate before the metal film deposition. However, sputtering-induced surface damage to the Ge was not annealed. Also, there was no direct evidence (such as Auger spectroscopy) to confirm that the sputtering actually had a net cleaning effect. Since sputter-deposition systems typically have relatively poor vacuum, the samples prepared probably contained at least monolayer coverage of contaminants at the time of film deposition.

In our experiments, we clean the substrate by low-energy ion sputter etching and thermal annealing in an ultrahigh vacuum (UHV) ambient. This technique for producing an atomically clean and ordered surface, although widely used in other fields, had not been used before in SPE experiments. This is partially because the sputter-anneal sequence to be completely effective as a cleaning technique, must be carried out in an ambient as free from reactive gases as possible. Otherwise, the substrate will be recontaminated after the sputtering is completed but before the ensuing film deposition can be initiated. This recontamination can be avoided by performing the deposition under UHV conditions.

Contaminants can also be introduced during metal or Si film deposition. In a vacuum evaporation system, there are several sources of these impurities. The simplest is gas atoms in the vacuum ambient. The flux of such atoms incident on the fresh film surface is approximately one monolayer per second for each 10^{-4} Pa (10^{-6} Torr) of pressure during the deposition. Since it is virtually impossible to determine the actual pressure in the vicinity of the substrate during film deposition, this parameter is usually not known. However, in our experiments the

evaporation source is thoroughly outgassed before the sample preparation sequence is begun. We have good evidence that films deposited in our system are free from contaminants to less than 500 ppm.

With respect to the purity of films deposited in previously reported SPE experiments, no data had been reported on this aspect of SPE until very recently. However, we now know that nearly all the reported results on growth in the Si crystal/Pd_2Si/Si amorphous system involved samples with substantially contaminated amorphous Si films.[9] The principal impurity detected in those experiments was carbon at a level of $\gtrsim$0.1 at.%. The source of C was thought to be the vitreous carbon crucible used to contain the Si charge during electron-beam evaporation of the amorphous films. A definite correlation between the level of C impurity and the growth rate and amount of trapped Pd in the grown layers has been noted.[10]

Most prior work on SPE involved exposing the sample to room air after the necessary thin films (e.g., Pd and Si) had been deposited. This was usually followed by heating in a vacuum furnace to induce silicide formation and Si SPE growth. Our work on UHV-deposited films indicates that the combination of exposure to room air and annealing furnace ambients can introduce surface and/or bulk contaminants that will impair the SPE growth process. Although we do not know whether room air exposure or furnace annealing is the critical step in SPE, both have the potential for introducing impurities on a large scale. For example, Auger electron spectroscopy (AES) shows that exposing a freshly deposited Si film to room air will produce a thin (10 to 20 Å) surface oxide layer containing adsorbed oxygen and hydrocarbons. During subsequent heating, these surface contaminants may be redistributed by diffusion into the bulk of the amorphous Si film. The impurity level due to this source could be substantial (e.g., $\sim$ 1 at.% for a 10 Å oxide on a 1000 Å Si film) if all the oxygen were incorporated in the film. It was recently shown that 1 at.% of either O or C can reduce the recrystallization rate of an amorphous Si layer to about 0.01 of the rate for uncontaminated samples.[11] Thus, the surface layer is a very potent source of contaminants in SPE when samples are exposed to room air prior to annealing.

Another important source of contamination is the residual background of gases within the annealing furnace. Even at 10^{-6} Torr, one monolayer per second is incident on the heated sample, providing the equivalent of roughly 10,000 Å of available contaminants hitting the surface of the sample during a 1-hr anneal. Of course, the incident atoms do not all stick on the surface, nor does the furnace ambient consist entirely of reactive gases. Nevertheless, the flux is considerable and is a potentially important source of contaminants. Recent work by Chang and Quintana[12] has shown that even inert gases in the furnace ambient must be considered in solid-state reactions. They found that the rate of diffusion of Au through Pt thin films is substantially increased in nominally inert (N_2, Ar) gas ambients in comparison with heating in vacuum. Although they were unable to identify the mechanism responsible for this effect, their findings emphasize the importance of considering all species of foreign atoms as potentially influential in low-temperature processes. The effect of inert gas atoms on SPE is, of course, an important consideration when film depositions are done in a sputtering system (as in the work of Ottaviani et al.[8]) or when heating is carried out in an inert gas furnace ambient.

In our work, the possible effect of contaminants introduced during annealing was minimized by performing the heating within the UHV chamber at pressures $\leq 2 \times 10^{-7}$ Pa. This is at least a factor of 100 improvement over typical vacuum furnaces and also avoids contamination from exposure to room air. As discussed below, processing completely under UHV has led to several results that had been unattainable by conventional processing methods. We are investigating the extent to which processing conditions can be relaxed while still obtaining good single-crystal epitaxy. This question is central in determining whether SPE can be made compatible with the production-line environment.

SECTION 3

EXPERIMENTAL APPARATUS

The goal of the first phase of our program, to establish the capability of growing films under uncontaminated conditions, was met by providing an UHV environment for all phases of the SPE growth process (i.e., substrate cleaning, film deposition, and crystallization). Since the vacuum system and fixtures assembled for this purpose were described in detail in Ref. 13, they will only be briefly summarized here.

In a typical SPE experiment, a combination of ion pumping, Ti sublimation, and LN_2 cryopumping are used to obtain pressures below 10^{-8} Pa. The Si substrates, mounted loosely on Ta pads, are cleaned by 2 kV Ar^+ bombardment and then heated to $\sim$900°C to produce an atomically ordered contaminent-free surface. AES and low-energy electron diffraction (LEED) are used to monitor surface cleanliness and crystallinity. Thin films are deposited from an electron-beam evaporator with unlined crucibles, using the highest purity source materials available. Conventional shadow masks and shutters define the deposition area on the sample, and film thicknesses are determined with a quartz crystal oscillator, calibrated by Dektak and Rutherford backscattering measurements.

Annealing to induce epitaxial layer growth can be performed within the UHV chamber by placing the sample close to a hot W disc. This method of heating results in uniform temperature distribution on the Si wafer, but limits determination of the absolute sample temperature to about ±25°C.

The chemical composition and crystallinity of the samples is analyzed after various stages of processing by Auger depth profiling and LEED. For more specific information on the orientation and crystallographic perfection of the samples after they are removed from the UHV system, we use Rutherford backscattering (RBS) channeling-effect measurements and, occasionally, glancing angle x-ray diffraction and transmission electron microscopy (TEM). Some samples also were examined by

scanning electron microscopy (SEM) combined with energy-dispersive x-ray (EDX) imaging.

To facilitate studying the effects of contaminants, our UHV system was equipped with a gas inlet system that can be used to admit controlled quantities of gaseous species at any stage of the SPE process. Additionally, to achieve a comparison with published work on non-UHV processing of SPE, a vacuum furnace was sometimes used for annealing and to induce silicide formation or epitaxial growth.

SECTION 4

RESULTS AND DISCUSSION

A. Si SPE WITH A Pd_2Si INTERLAYER: UNCONTAMINATED

In studying the SPE of Si in the system Si(crystal)/Pd_2Si/Si(a), we used two slightly different sequences of film depositions and heatings to form the initial sample structures. In one, the silicide interlayer is formed after both the Pd and amorphous Si films are deposited. In the other, the silicide reaction is carried to completion before the Si layer is deposited. We will refer to the former sequence as "conventional" since it is the process employed in all previously published work. The other sequence will be called "pre-silicided" since the silicide is formed prior to amorphous Si deposition. The latter process was used in most of our work on uncontaminated samples. In some instances, however, a direct comparison between the two processing sequences was made, and the results are discussed where appropriate.

The pre-silicide process can only be implemented in an oxygen-free deposition system equipped with a sample heater, since forming the Pd_2Si layer in an oxygen-containing ambient will produce a silicon-oxide layer at the uncovered silicide surface. If Si is deposited onto such an oxidized surface and the sample is heated, SPE will not occur. The oxide presumably inhibits the transport of Si through the silicide and thus interrupts the supply of Si atoms to the growth interface. Fortunately, in UHV the silicide can be formed with no detectable surface oxidation.

For most of our experiments on SPE using Pd_2Si, both (100)- and (111)-oriented Si substrates were tried. For samples processed entirely in UHV, no gross differences in the behavior of SPE on the two substrate orientations were observed. As discussed in more detail below, this insensitivity to substrate orientation is in sharp contrast with other reports of SPE using Pd_2Si (Ref. 14) where homoepitaxial growth could not

be achieved for the (111) orientation. It is not known whether this radical difference in behavior for (111)Si substrates is primarily the result of different contaminant levels or the difference in processing sequence (pre-silicide versus conventional treatment).

In Figure 2 we have illustrated the pre-silicided process used in experiments to determine the nature of SPE performed under uncontaminated conditions. The surface layer after growth consists of a mixture of Pd_2Si and Si, rather than a pure layer of Pd_2Si. This finding represents a major point of departure of our results on clean SPE compared to previous non-UHV work on SPE using Pd_2Si. Next we present data from various analyses which help to define the nature of the SPE samples processed in UHV.

In-depth composition profiles showing the outcome of SPE under non-contaminated conditions were obtained by a combination of AES and ion sputter-etching. Typical results for a <111>Si substrate are presented in Figure 3. To arrive at the atom fractions of Si and Pd shown in the figure, the raw Auger derivative peaks were individually normalized to the signals from pure standards of freshly deposited Pd and Si films in UHV. The conversion of sputter time to depth in the specimen was done by independent Rutherford-backscattering analysis of the sample. Comparison of the upper and lower panels of Figure 3 shows that annealing causes an interchange of Pd_2Si and amorphous Si layers, indicating that SPE has occurred. But after SPE growth, the region containing Pd_2Si is about 50% thicker than the original silicide layer, and the Pd atom fraction is only 43%, instead of 67% for pure Pd_2Si. One possible interpretation of this result is that the outermost layer is not laterally homogeneous, but consists instead of regions of Pd_2Si interspersed with regions of Si. This has been confirmed by a combination of SEM, RBS, and LEED analyses (discussed below).

Figure 4 presents SEM micrographs of SPE samples processed entirely in UHV. Figure 4(a) shows the surface of an Si <111> SPE sample that had been heated for 8 hr at 525°C in UHV. The white areas in the upper

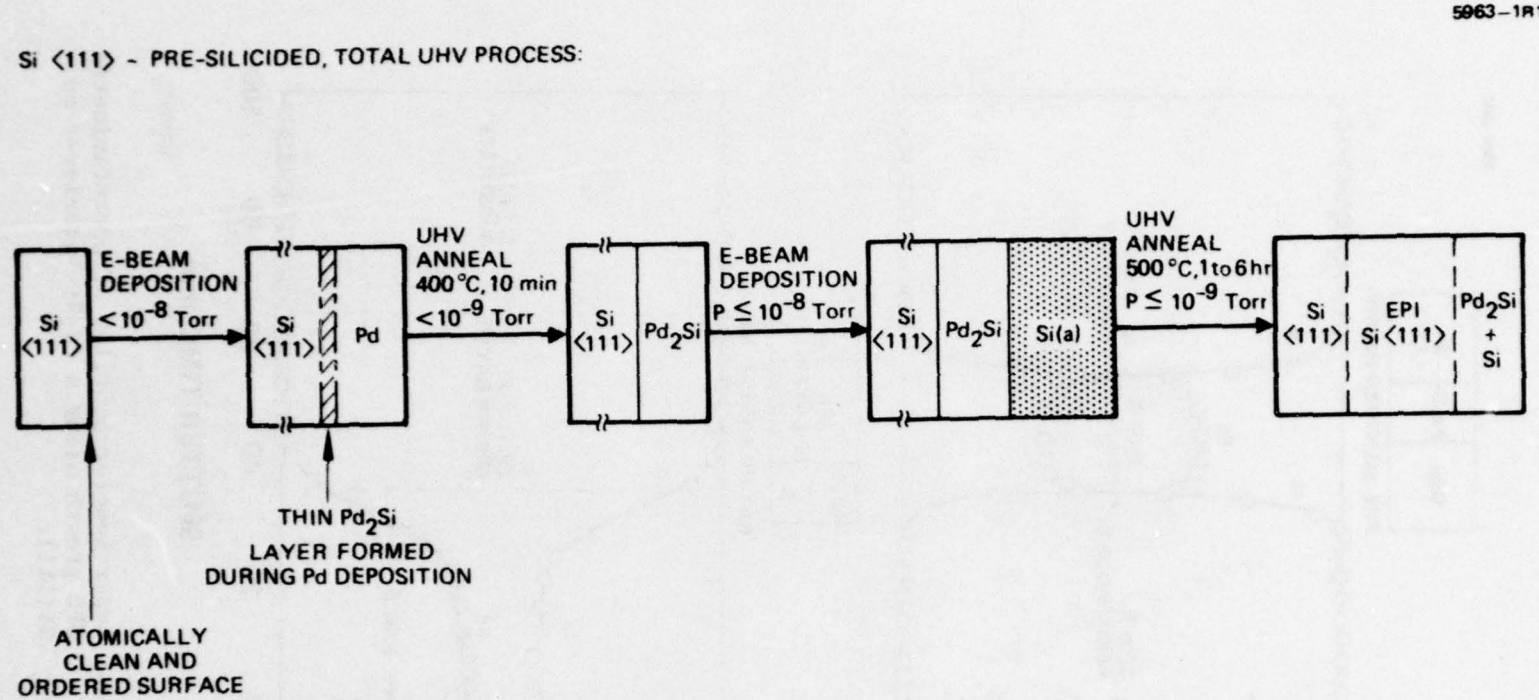

Figure 2. Illustration of the "pre-silicide" process for SPE growth of Si in UHV.

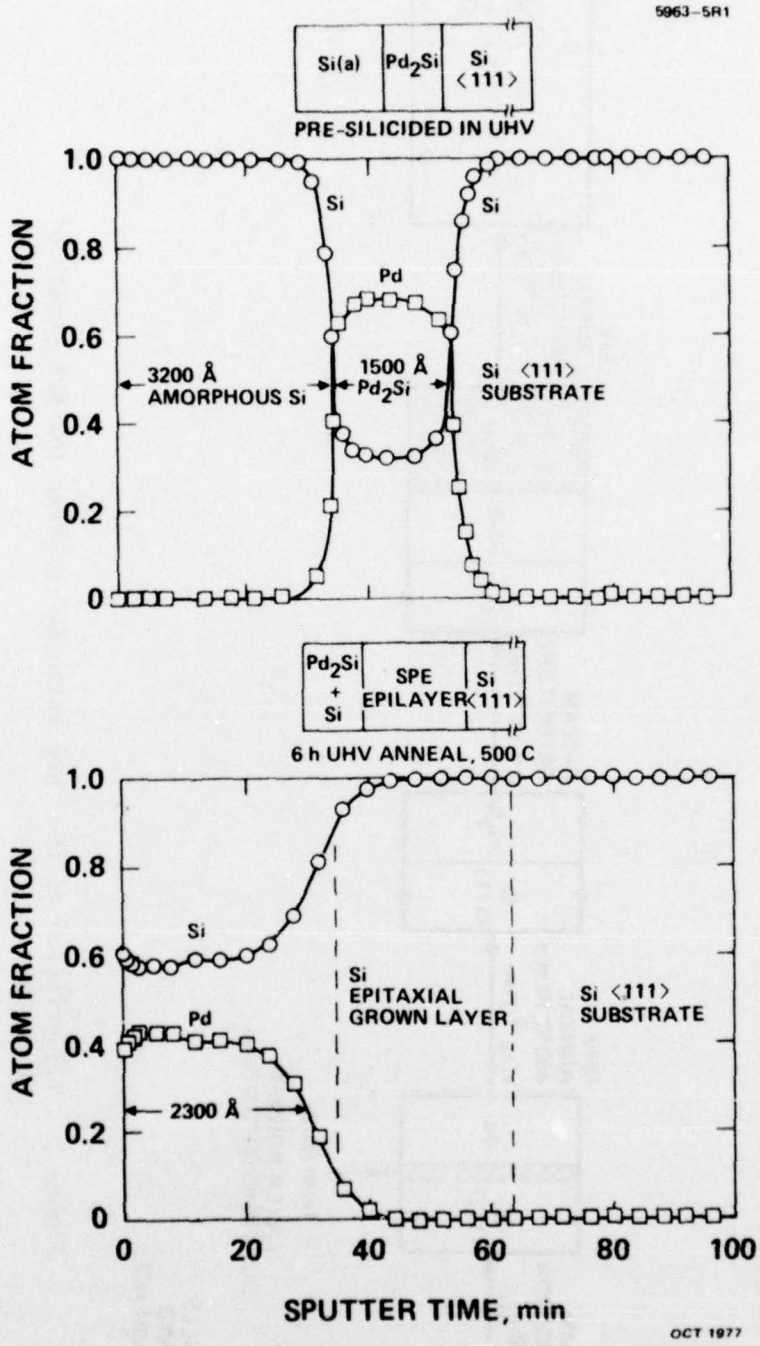

Figure 3. Auger sputter profiles of uncontaminated SPE growth using a Pd_2Si interlayer on Si(111).

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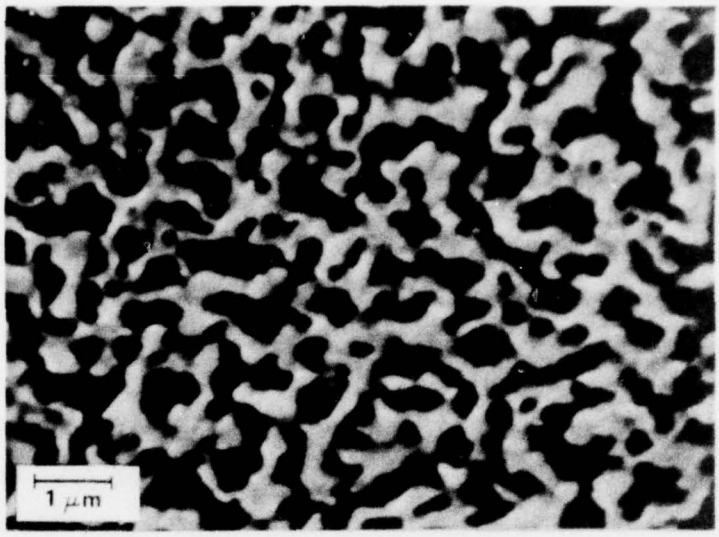

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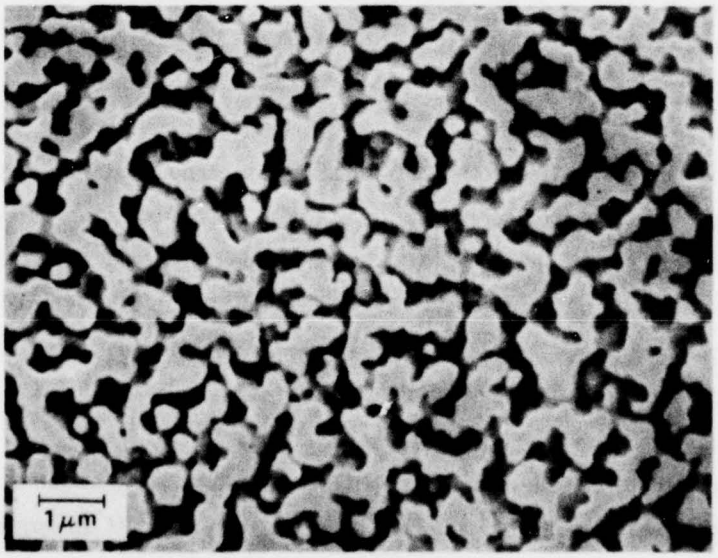

b) Pd_2Si REMOVED BY ETCHING

Figure 4. SEM micrographs of the surface of a UHV-processed SPE sample after growth.

photo were shown (by energy-dispersive X-ray imaging) to contain Pd; the dark areas were shown to be pure Si. Thus, the light areas must consist of Pd_2Si since the occurrence of free Pd is highly unlikely considering that the sample had been subjected to long-term heating.

The micrograph in Figure 4(b) was taken after the sample had been etched briefly in aqua regia to remove the Pd_2Si. The large pits left by the etching show that the Pd_2Si had been totally interspersed with the Si in this sample after SPE growth. This explains the low Pd fraction indicated by Auger profiling: since the area analyzed with our Auger instrument was at least 2500 times that shown in the SEM micrographs, the Pd fraction is deduced from a lateral averaging over Pd_2Si and Si regions.

To find out how deeply the Pd_2Si penetrates beneath the surface of the UHV SPE samples, 2 MeV RBS analysis has been performed. An RBS spectrum of the sample shown in the SEM photos is presented in Figure 5. For comparison, we have also included a solid line showing how the spectrum would have looked if the Pd_2Si layer (originally 1350 Å thick, beneath 3700 Å of amorphous Si) had been uniformly displaced to the surface during growth. By carefully considering the relationship between energy loss and depth for Si and Pd_2Si, we showed that the Pd_2Si regions extend to $\sim$3160 Å below the surface, which leaves about 1540 Å of grown Si free of undetectable Pd. This Pd-free region was also examined by AES depth profiling, where the sensitivity for Pd is about 0.05 at.% and no Pd has been detected.

Thus, SPE carried out under clean conditions produces a grown layer slightly thicker than the original Pd_2Si layer. Pd trapping in this layer is below 0.05 at.%. This finding is common to all UHV-processed samples so far examined, whether <100> or <111> oriented. The sample beyond the Pd-free region consists of spires, or columns, of Si leading to the surface and surrounded by Pd_2Si. Examination with RBS channeling-effect and LEED measurements of this outer region showed that the Si is everywhere epitaxial in spite of the complicated topography.

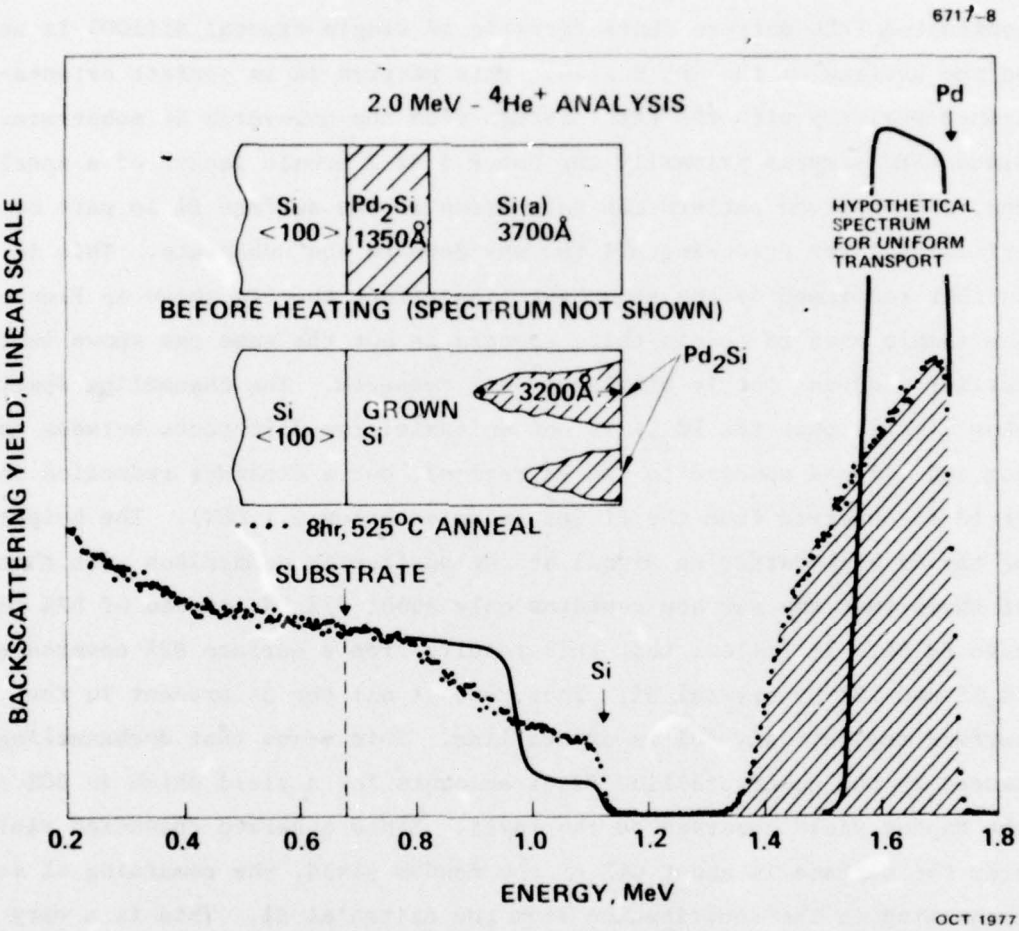

Figure 5. Backscattering spectrum from a Pd_2Si-interlayer SPE sample grown in UHV.

Figure 6 gives evidence that the Si in non-contaminated SPE samples is epitaxial. The Pd_2Si on Si(100) does not exhibit a LEED pattern, which indicates that long-range order is lacking. However, a well-contrasted LEED pattern characteristic of single-crystal Si(100) is seen on the surface of the SPE region. This pattern is in perfect orientational registry with the LEED pattern from the uncovered Si substrate. Since LEED samples primarily the outer 1 or 2 atomic layers of a specimen, the observed pattern can only arise if the surface Si is part of an epitaxial layer extending all the way down to the substrate. This is further confirmed by the RBS channeling-effect spectra shown in Figure 7. The sample used to obtain these spectra is not the same one shown in the earlier figures, but is similar in all respects. The channeling spectra show clearly that the Pd_2Si is not epitaxial (no difference between random and aligned spectra in the Pd region), but a distinct reduction in yield is observed from the Si (at energies below 1.1 MeV). The height of the Pd backscattering signal at the surface in comparison with that of Si shows that the surface contains only about 55% Pd instead of 67% for pure Pd_2Si. It follows that this results from a surface 82% covered by Pd_2Si and 18% by crystal Si. Thus, out of all the Si present in the surface region, only 40% is crystalline. This means that dechanneling caused by the noncrystalline Pd_2Si accounts for a yield which is 60% of the random yield observed on the layer. Since observed channeled yield near the surface is about 64% of the random yield, the remaining 4% dechanneling is the contribution from the epitaxial Si. This is a very respectable figure, and it shows that within experimental error, the Si has good epitaxial crystallinity all the way to the surface, as had been indicated by LEED analysis.

Given, then, that SPE in uncontaminated samples causes epitaxial Si protuberances that reach the surface, what is the significance of this finding? Referring to the schematic of SPE on (100)Si shown in Figure 6, it is apparent that epitaxial growth of Si occurs both where there is Pd_2Si and in regions where amorphous Si is in direct contact with the

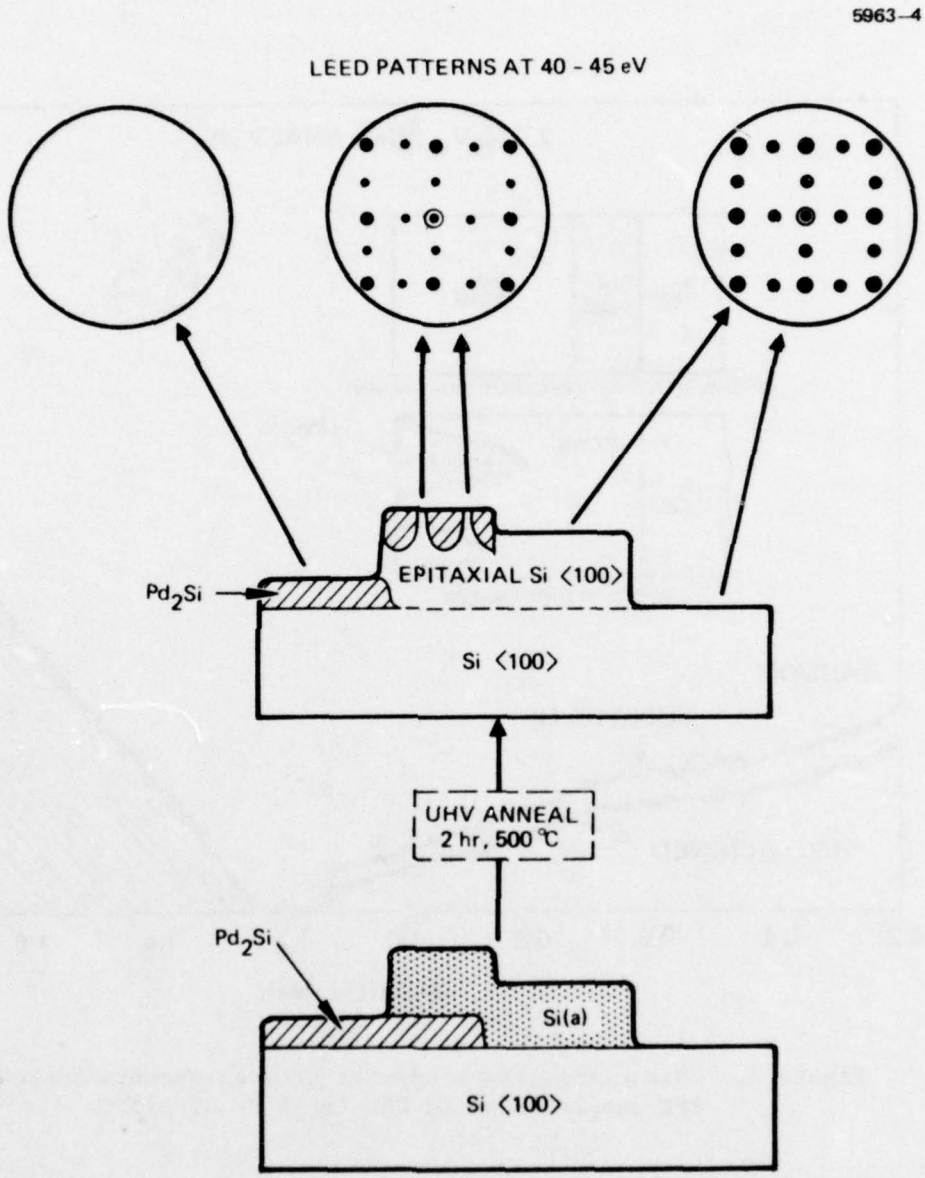

Figure 6. Behavior of SPE samples during UHV processing.

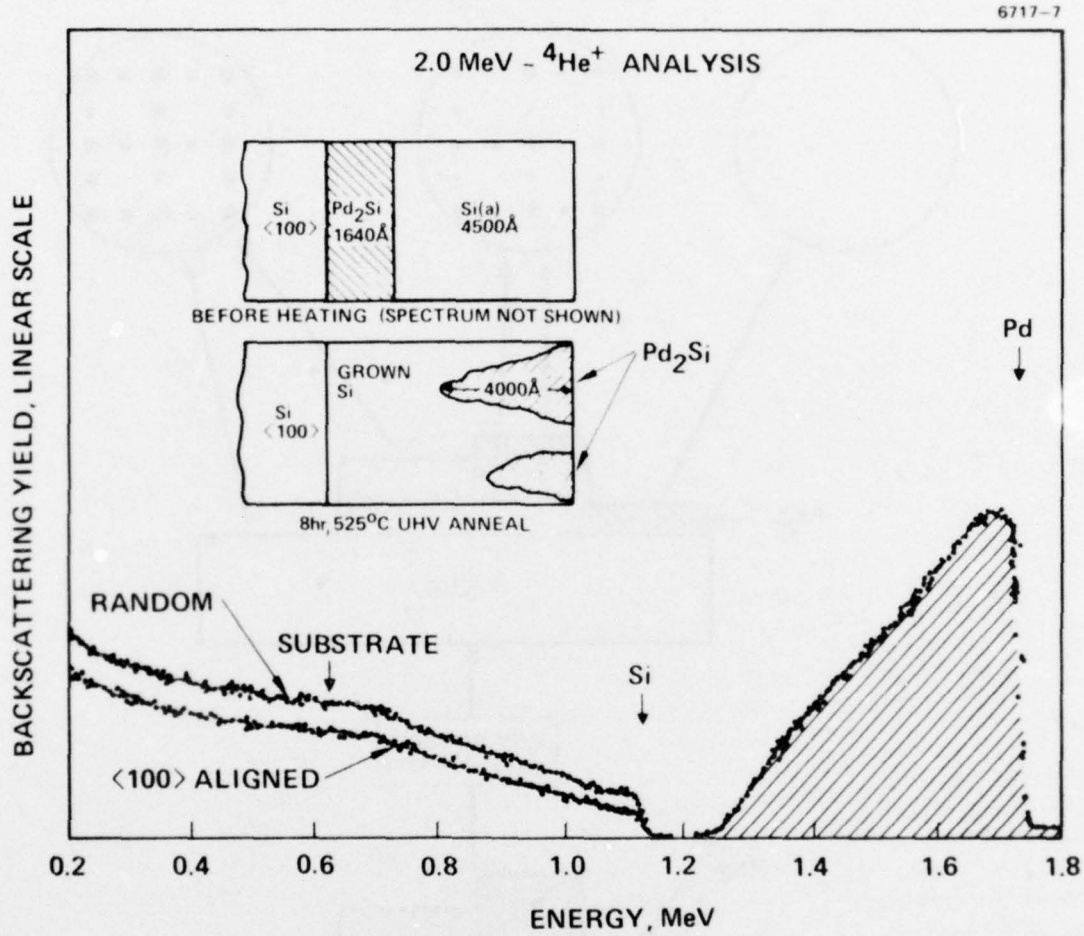

Figure 7. Channeling-effect spectra from an uncontaminated SPE sample grown in UHV for 8 hr at 525°C.

crystalline substrate. This result (discussed in greater detail below) demonstrates that the tendency of amorphous Si to form a single-crystal layer is very strong when contaminants are absent. This raises the possibility that Pd_2Si might actually obstruct the crystallization process in contaminant-free specimens. That is to say, given clean enough conditions, amorphous Si will grow epitaxially on a single-crystal substrate. Thus, for samples having a Pd_2Si interlayer, once a gap is opened in the silicide, crystallization may proceed quite rapidly, forming columnar regions that reach to the surface. Quite possibly, the initial stage of growth prior to silicide breakup consists of nucleation and island formation similar to the "first transient" growth stage envisioned by Liau.[15] However, the Pd_2Si layer must develop "holes" at some time during heating to explain the growth out to the surface that we described above. The growth of columnar "grains" through openings in the Pd_2Si may occur simultaneously with a dissociative growth mechanism (as suggested in Ref. 16) that operates in regions still covered by Pd_2Si. In fact, some mechanism of this type must occur to account for the displacement of the Pd_2Si to the surface. Without such a mechanism, the lateral development of the columnar grains would be expected to cause the entrapment of the silicide below the surface (which is contrary to the experimental findings).

This explains why the ratio of Pd_2Si to free Si in the surface layer of SPE samples does not approach the pure Pd_2Si ratio as anneal time increases. Once all free Si in a sample has been crystallized epitaxially (including columnar protuburances), the overall free energy of the sample is very nearly minimum. Thus, the rate of conversion to a uniform Pd_2Si layer sitting atop a uniform Si single crystal will be extremely slow. Thus, a surface mixture of Pd_2Si regions and epitaxial Si regions is effectively a stable state.

Further investigation into the mechanisms of growth in uncontaminated SPE using Pd_2Si is needed. By varying the growth temperature, it might be possible to reduce the rate of columnar Si crystallization to

considerably below the rate of the parallel process of "Pd_2Si displacement" growth. This would presumably favor the uniform displacement of Pd_2Si to the surface and result in a final configuration closer to the published results on contaminated SPE,[3] but without trapped Pd in the epitaxial Si layer. The early stages of columnar growth should be observable by LEED analysis once enough columns reach the surface. This kind of analysis could be used in conjunction with Auger depth profiling to determine the effect of growth temperature on the balance between the different processes.

The growth of much thicker layers than those examined so far also should be studied. It is possible that a thickness limit exists beyond which the lateral growth of columns would result in entrapment of Pd_2Si beneath the surface.

Finally, the study of contaminant effects on the characteristics of SPE growth has just begun, and will certainly provide additional insight into the mechanisms responsible for the wide variety of behavior seen in samples processed under different conditions. In particular, we want to understand why samples prepared under contaminated conditions sometimes exhibit uniform layer growth[15] without the Pd_2Si layer losing its physical continuity, whereas in uncontaminated samples the Pd_2Si is penetrated by Si islands, which lead to nonuniform, columnar growth. Results discussed in the following sections indicate that contaminants can penetrate an amorphous Si film during room air exposure or furnace annealing, and thus may also be incorporated into the Pd_2Si layer during its formation. It is possible, therefore, that the PD_2Si layer itself plays a crucial role in determining the effects of contaminants on SPE growth in the $Si/Pd_2Si/Si(a)$ system.

B. METAL-FREE SPE

As previously noted, SPE crystallization of amorphous Si films has been observed on (100)Si that lacked a metallic interlayer (cf. Figure 6). This has been replicated several times, even with samples on which no Pd_2Si whatsoever was present. This leads to the conclusion that, in the absence of impurities, there are no significant energy or kinetic barriers to the single crystallization of amorphous Si on (100)-oriented

substrates. In retrospect, this conclusion seems intuitively obvious, since it is what one would expect based on simple considerations of free-energy gain as a "driving force." However, practical problems, particularly the presence of contaminants, greatly complicated the demonstration of this "simple" result. With one exception (Jona's[17] work on 10 to 15 Å films), we know of no other instance in which the direct epitaxial crystallization of deposited Si films has been observed.

Metal-free SPE provides the ideal situation in which to begin a study of contaminant effects, since even the metallic interlayer has been removed as a possible contaminant. Consequently, we are presently devoting considerable attention to this growth process. Initial experiments have focused mainly on determining the crystallographic quality of epitaxial layers grown by this method. Details of the work performed so far in this area are presented in Appendix A.

The principal conclusions of our work on metal-free SPE are that epitaxial layers exhibiting a high degree of crystallographic perfection can be grown by heating amorphous Si films to about 500 to 600°C in UHV. The growth rates observed on (100)Si substrates are consistent with the rate of recrystallization of ion-implanted layers,[18] which suggests a similar growth mechanism. Neither deposition rate of the amorphous film nor temperature control during growth seems to be important to the achievement of epitaxy. Impurity effects, on the other hand, appear to be critical. To demonstrate the effect of contaminants, samples were prepared in UHV but removed for annealing in a vacuum furnace ($P \leq 5 \times 10^{-5}$ Pa). After 9 hr heating at 525°C, examination by 280 keV He^{++} channeling showed no evidence of epitaxial crystallization. Similar samples annealed in UHV usually crystallize completely in 1 to 2 hr. Evidently, either the exposure to room air during transfer to the furnace or the background contaminants in the furnace ambient is sufficient to inhibit the crystallization process. Experiments are in progress to isolate the critical contaminant and to identify the processing step in which it is introduced. It is clear, however, that substantial penetration of the amorphous layer by contaminant atoms must be occurring

to explain the lack of epitaxial crystallization. If only the surface were affected by contaminants we should still have observed channeling in the underlying epitaxial layer, but none was observed.

The disruption or inhibition of epitaxial growth also has been observed for Pd_2Si interlayer samples removed from UHV for furnace annealing. Although the metal-free samples seem more sensitive to this type of handling, the effects on Pd_2Si SPE nevertheless are dramatic, and are reviewed in the following section.

C. EFFECTS OF ROOM AIR EXPOSURE AND/OR VACUUM FURNACE ANNEALING

As already mentioned, metal-free SPE samples fail to crystallize epitaxially if transferred from UHV to a vacuum furnace for annealing. Similar behavior has been observed with Pd_2Si interlayer samples prepared by the nonpresilicided process and annealed in a vacuum furnace. In this type of sample, a large fraction of the Pd_2Si layer remains near the original Pd_2Si/amorphous Si interface instead of being displaced to the surface during annealing. This is shown schematically in Figure 8 and illustrated by RBS spectra in Figures 9 and 10. There is a very fundamental difference between the "split" distribution of Pd found in the conventionally processed sample shown in Figure 9 and the gradual tapering of Pd_2Si regions found in the uncontaminated SPE samples discussed earlier (see Figure 5). This difference is more easily appreciated by referring to the RBS spectrum in Figure 10. This spectrum was obtained after removing the outer Pd-containing surface region by using ion sputter-etching. The figure shows that the buried Pd distribution is physically separate from the surface distribution, as evidenced by the very low Pd concentration at the surface of the ion-milled specimen.

The grown Si layer is mostly polycrystalline when clean Si/Pd/Si samples are annealed in a vacuum furnace. However, good epitaxial growth can be reproducibly obtained on furnace-annealed specimens if C is introduced into the amorphous Si layer during deposition.[9] This finding combined with the data of Kennedy et al.,[11] which shows that C impurities decrease the crystallization rate of amorphous Si, led to the

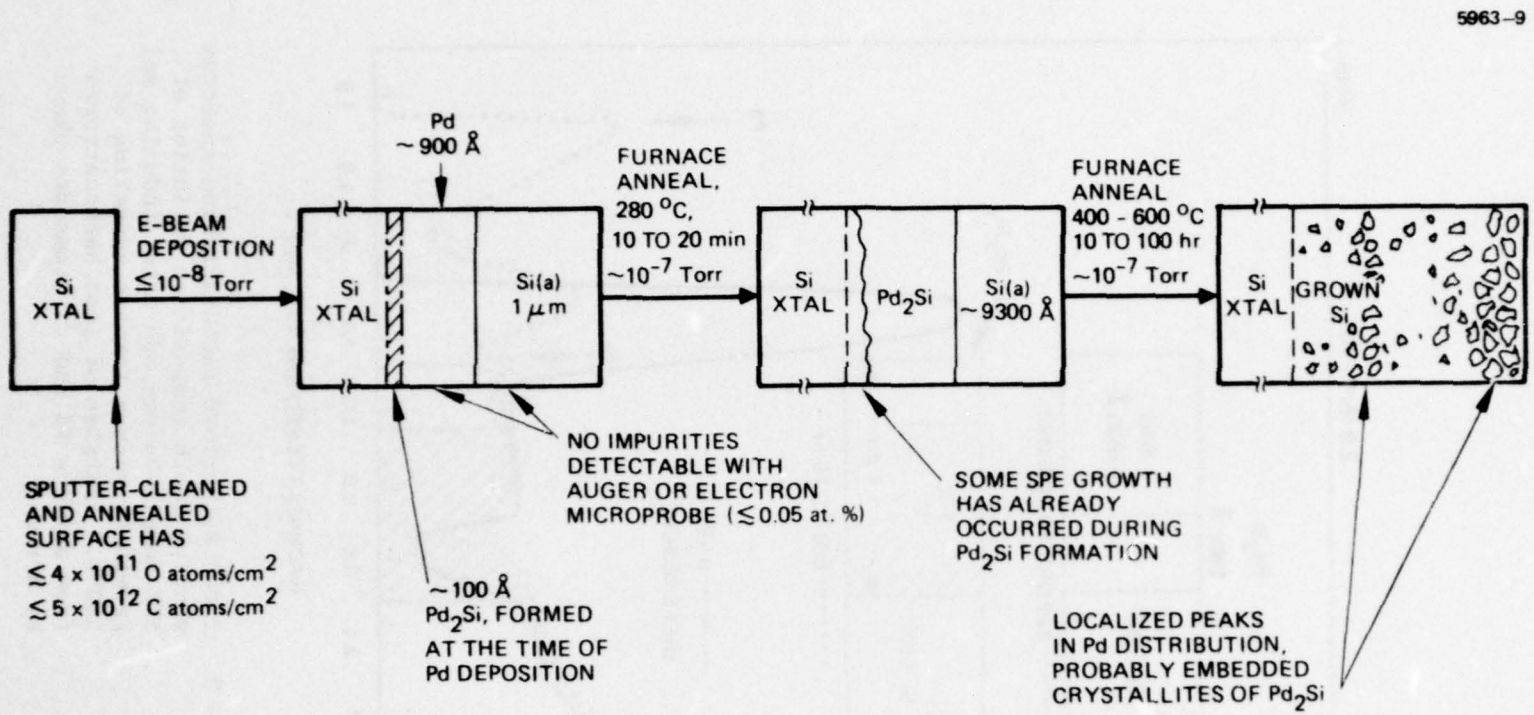

Figure 8. Depiction of SPE process showing behavior of non-pre-silicided samples annealed in a vacuum furnace.

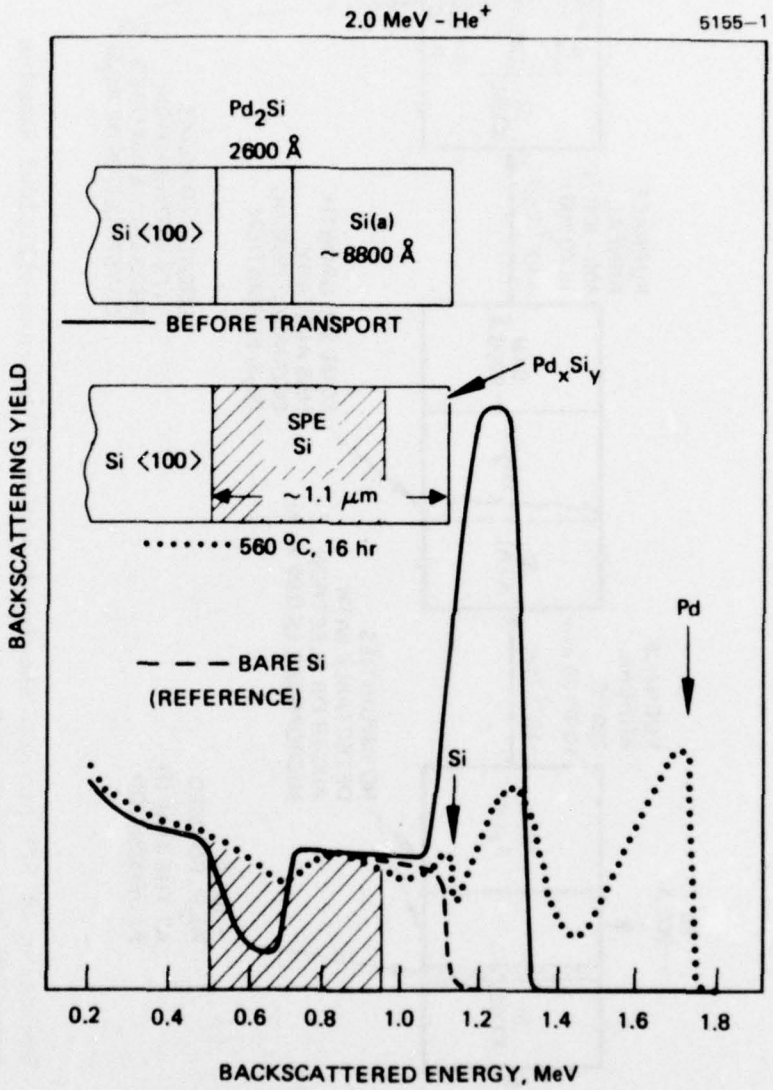

Figure 9. 2 MeV Rutherford backscattering spectrum showing depth composition variation of SPE sample before and after inducing epi growth by vacuum furnace annealing at 560°C. Energies of ions backscattered from surface Pd and Si atoms are shown by arrows.

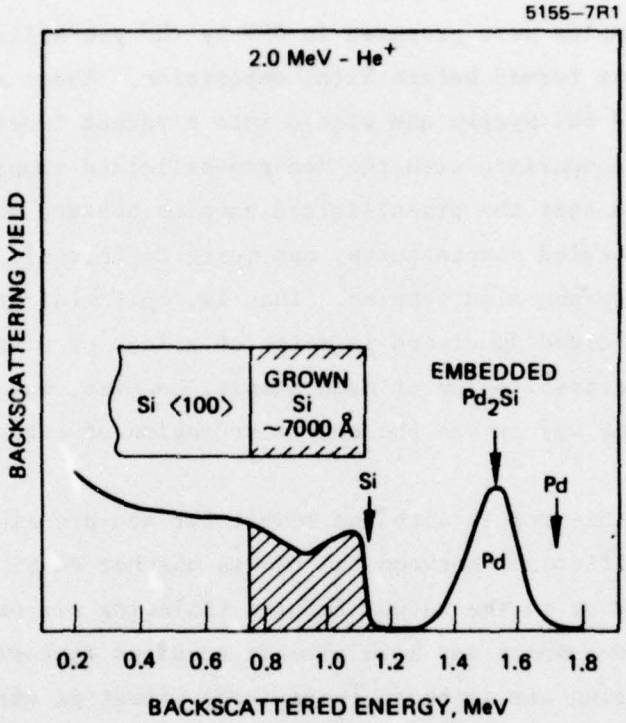

Figure 10. Same conditions as dotted curve of Figure 9, but with ~4500 Å removed from surface by sputter etching with Ar^+ ions to expose the embedded Pd_2Si distribution.

suggestion[9] that C may affect SPE growth by inhibiting premature crystallization of the amorphous Si layer before or during the desired transport process. In this model, C acts to slow down the unwanted process of crystallization within the amorphous Si layer sufficiently to allow the desired (transport) process to dominate. We recently performed experiments, however, that indicate that this effect is not in itself sufficient to explain the effect of C on SPE.

Several samples were prepared in UHV by the pre-silicide process in which Pd_2Si is formed before Si(a) deposition. These samples were removed from the UHV system and placed into a vacuum furnace for annealing to allow a comparison with the non-pre-silicided samples discussed above. We found that the pre-silicided samples behaved very similarly to their UHV-annealed counterparts, but quite differently from non-pre-silicided furnace-annealed samples. That is, epitaxial growth occurred for the pre-silicided specimens in spite of a lack of C in the Si(a) layer. The outermost region of each sample, however, was laterally mixed in the same way as was the outermost region of each total UHV sample.

Comparing this result with the result for non-pre-silicided samples the principle difference between the two is whether Pd_2Si formation is performed in UHV or in the vacuum furnace following air exposure. Since furnace-annealed samples may have already acquired contaminants in the amorphous Si during air exposure (recall the effect of air exposure on metal-free SPE), there is a good chance that these contaminants may be incorporated into the Pd_2Si layer during the silicide reaction. Samples pre-silicided in UHV, however, contain a contaminant-free Pd_2Si layer. Thus, the different behavior of the two types of SPE samples might be explainable in terms of different silicide properties caused by contaminants in the amorphous region.

One particularly important question is how C can offset the deleterious effect of the other contaminants introduced during air exposure. Although the question remains unanswerable, there is a crucial difference in the behavior of C-free versus that of C-containing samples: the

apparent cohesiveness of Pd_2Si in the latter. That is, the Pd_2Si interlayer does not appear to lose its structural continuity in C-containing samples, but clearly breaks up in the nominally contaminant-free or C-free samples. Therefore, it appears that a particularly important area to investigate is the effect of C in Pd_2Si on the silicide microstructure and physical properties. One way to approach this issue experimentally would be to ion-implant C into a Pd_2Si layer on Si, then return the sample to UHV for clean Si deposition and subsequent transport. If the Pd_2Si fails to break up under these conditions, the effect of C would be clearly established. The next step would then be to find out whether C goes into the grain boundaries or other sites in the Pd_2Si. This type of experiment is presently being pursued.

SECTION 5

PLANS FOR FUTURE WORK

We will continue to study the growth of Si by metal-free SPE to determine the effect of contaminants on the process. Two particularly important questions are how contaminants enter the amorphous Si film after the samples are removed from the UHV system and how the crystallization process is inhibited. There seems to be a discrepancy between our findings on deposited amorphous Si and those of other workers on crystallization of ion-implanted amorphous layers. The other work did not find that exposure to room air and furnace annealing inhibited crystallization whereas we have been unable to obtain crystallization of deposited films under nominally identical conditions. It is extremely important to understand this apparent difference in susceptibility to contaminants, since it would obviously be much more convenient to anneal samples in a vacuum furnace than within the UHV system.

We also hope to soon begin to grow doped layers by the metal-free SPE process. This will probably be accomplished initially by using a doped Si source in the electron-beam evaporator, instead of the high-purity Si presently in use. Alternatively, it may be desirable to install a separate source of dopant atoms in the UHV system.

In the area of SPE with Pd_2Si interlayers, we plan to continue studying UHV-prepared samples. Since the results obtained so far seem to indicate that the Pd_2Si interlayer plays a key role in determining the susceptibility of the interlayer SPE process to contaminant effects, we will begin looking more specifically at the properties of the silicide. Intentional introduction of impurities into the Pd_2Si will be investigated. We will also examine how contaminants present in the amorphous Si layer may be incorporated in the Pd_2Si when the silicide is formed while covered by Si(a), as in the conventional process. It will probably be necessary to use SIMS analysis for several of these studies, since C

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cannot be detected by AES in the presence of Pd because of the unfortunate overlap of their spectral features.

In view of the complexities of behavior already found in SPE with Pd_2Si interlayers, it does not seem prudent for us to investigate other interlayer systems at this time.

REFERENCES

1. J.A. Roth and C.L. Anderson, to be published in Appl. Phys. Lett., 15 Nov. 1977.

2. C. Canali, J.W. Mayer, G. Ottaviani, D. Sigurd, and W. Van der Weg, Appl. Phys. Lett. 25, 3 (1974).

3. C. Canali, S.U. Campisano, S.S. Lau, Z.L. Liau, and J.W. Mayer, J. Appl. Phys. 46, 2831 (1975).

4. H. Sankur, J.O. McCaldin, and J. Devaney, Appl. Phys. Lett. 22, 64 (1973).

5. J.E. Davey, A. Christou, and H.M. Day, Appl. Phys. Lett. 28, 365 (1976).

6. C. Canali, J.W. Mayer, G. Ottaviani, D. Sigurd, and W. Van der Weg, Appl. Phys. Lett. 25, 3 (1974).

7. A. Christou, J.E. Davey, H.M. Day, and H.B. Dietrich, Appl. Phys. Lett. 30, 598 (1977).

8. G. Ottaviani, C. Canali, and G. Majni, J. Appl. Phys. 47, 627 (1976).

9. Z.L. Liau, S.S. Lau, M-A. Nicolet, J.W. Mayer, R.J. Blattner, P. Williams, and C.A. Evans, Jr., Proceedings of the Third International Conference on Ion Beam Analysis, Washington, D.C., 1977, Nucl. Inst. and Meth.

10. Z.L. Liau, private communication.

11. E.F. Kennedy, L. Csepregi, J.W. Mayer, and T.W. Sigmon, Appl. Phys. (to be published).

12. C.C. Chang and G. Quintana, Appl. Phys. Lett. 29, 453 (1976).

13. C.L. Anderson and J.A. Roth, "Solid Phase Epitaxial Growth," Annual Progress Report, Contract N00014-75-C-0957, Office of Naval Research.

14. S.S. Lau, Z.L. Liau, M-A. Nicolet, and J.W. Mayer, J. Appl. Phys. 48, 917 (1977).

15. Z.L. Liau, S.S. Lau, M-A. Nicolet, and J.W. Mayer, Thin Solid Films 44, 149 (1977).

16. R. Pretorius, Z.L. Liau, S.S. Lau, and M-A. Nicolet, Appl. Phys. Lett. 29, 598 (1976).

17 F. Jona, Surfaces and Interfaces, J.J. Burke, N.C. Reed, and V. Weiss, Eds. (Syracuse U.P., Syracuse, 1967).

18. L. Czepregi, J.W. Mayer, and T.W. Sigmon, Phys. Lett. A54, 157 (1975).

APPENDIX

Silicon Epitaxy by Solid-Phase Crystallization of Deposited Amorphous Films[a]

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ABSTRACT

We report the solid-phase growth of epitaxial Si thin films by the heating of amorphous Si deposited onto atomically clean (100)Si substrates at room temperature. Epitaxial Si layers ranging in thickness from 1000 to 5000 Å have been grown by heating the amorphous films in ultrahigh vacuum to temperatures of 500 to 600°C. Good crystal quality of the layers grown by this method has been demonstrated by Rutherford backscattering and transmission electron microscopy.

[a]Work supported by the Office of Naval Research.

Interest in solid-phase growth of epitaxial Si layers for device purposes arises primarily from the low temperatures used (400 to 600°C) compared to conventional epitaxial growth techniques (e.g., silane pyrolysis), which use temperatures in the 900 to 1200°C range.[1] Because the diffusivity of common dopants and of lifetime-degrading impurities is reduced during growth at low temperatures, low-temperature processes are advantageous for the production of extremely thin, uniform epitaxial layers with abrupt doping profiles. An important application for epitaxial Si having these properties is in the field of microwave devices, where the desire to achieve higher frequency operation dictates using submicron-thickness active layers with abrupt doping changes at layer boundaries. The growth of such layers by high-temperature epitaxial techniques is extremely difficult because of dopant interdiffusion during growth as well as the problems associated with growing thin layers at high growth rates.[1] Solid-phase epitaxy (SPE), by virtue of its lower temperatures and implicit thickness control, has the potential for eliminating these difficulties.

Ideally, SPE should be possible by depositing an amorphous film onto a single-crystal substrate, then annealing to cause the deposited film to be converted into a monocrystalline layer in registry with the substrate. The basic "driving force" for such a reaction is the lower free energy of the ordered single-crystal compared to the amorphous state. However, heating an amorphous Si film which has been deposited onto a typical single-crystal wafer will not produce this result. The native oxide and other contaminants present on the substrate surface before film deposition remain at the substrate/film interface and

obscure the crystalline "template." When such a specimen is heated, nucleation and growth of individual grains occur independently, without orientational coherence between grains. This produces at best a polycrystalline film. Thus, one prerequisite for successful SPE is the removal of contaminants from the substrate.

In previously published reports of successful Si growth by SPE, removal of substrate contaminants has been achieved through using a metal film deposited onto the substrate before the Si deposition.[2-5] This metal-interlayer approach, although effective in generating an adequate growth interface for SPE, unfortunately produces epitaxial layers heavily contaminated (> 0.1 at.%) with metal atoms from the interlayer.[2-5] Since this background of metal impurities would seriously limit the utility of such layers for device applications, it is highly desirable to find an alternative to the metal-interlayer approach.

In this paper, we show that epitaxial Si layers can be grown by SPE without a metal interlayer, provided that the substrate surface is properly prepared in an atomically clean and ordered condition (using ultrahigh vacuum (UHV) processing) before the amorphous Si film is deposited. By annealing Si films to temperatures in the 500 to 600°C range, we have grown 1000 to 5000 Å epitaxial layers having low defect densities. Furthermore, the growth process used does not appear to require precise temperature or deposition rate control. Epitaxial layer thickness is determined solely by the thickness of the deposited amorphous film, which can easily be controlled by conventional techniques.

In this work, substrates of 0.2 Ω-cm p-type, boron-doped, float-zone (100) Si were chemically cleaned, then loaded into a UHV chamber. After bakeout of the vacuum system, a base pressure of $<10^{-8}$ Pa was achieved. Oxide and hydrocarbon contaminants were removed from the Si surface by sputter-etching with 2 keV Ar^+ ions at near-normal incidence for a time sufficient to remove ~50 Å of Si. Sputter-cleaning damage was annealed by heating the samples to approximately 900°C for 2 min. The surfaces produced in this manner exhibit a Si(100)-2 LEED pattern, and have been verified to be free of contaminants to below 0.001 monolayer by Auger electron spectroscopy (AES).

Si was deposited onto the atomically clean and ordered substrates by electron-beam evaporation at rates varying from 5 to 25 Å/sec. The evaporant source material was polycrystalline Si of the highest available purity. Vacuum system pressure during deposition was below 10^{-6} Pa. The films prepared under these conditions were free of contaminants as measured by AES.

Epitaxial crystallization of the deposited films was induced by heating the samples in the UHV chamber to a temperature in the 500 to 600°C range. During this heating, the system pressure stayed below 2×10^{-7} Pa. This minimized the possibility of impurity indiffusion during growth. Heating for 1 to 2 hr was usually sufficient to cause complete epitaxial crystallization of Si films 1000 Å to 5000 Å thick.

Information concerning the degree of crystallographic perfection of metal-free SPE films was obtained by transmission electron microscopy (TEM) and Rutherford backscattering (RBS) channeling-effect analysis.

In Figure 1, we present RBS channeling spectra from a 4500 Å Si layer grown on (100) Si by heating for 2 hr at 525 ± 25°C (as described above). The solid dots are the backscattering yield for random incidence of the $^4He^+$ analysis beam, and the open circles are the channeling yield obtained with the beam aligned parallel to a substrate [100] direction. The large reduction in backscattered yield caused by channeling of the He^+ beam (~25:1 channeling dip) is strong evidence for the epitaxial orientation of the grown film. In contrast, epitaxial Si films grown by the metal-interlayer method typically exhibit a channeling dip of only ~14:1 (Ref. 3). This comparison shows the improved crystallinity achieved by the present technique. Indeed, channeling data for the grown layer shown in Figure 1 are identical to spectra taken on an exposed portion of the single-crystal substrate.

TEM analysis also indicated the quality of the layers grown by metal-free SPE. Figure 2 shows a bright-field micrograph from a typical area on a (100) Si epitaxial film and the corresponding selected-area diffraction pattern. The micrograph shows several groups of straight dislocations of approximately equal length and numerous very small blemishes of unknown origin. Detailed examination of the dislocation images has shown that they originate at or near the substrate/film interface and extend through the epitaxial layer, inclined relative to the surface normal. This type of behavior is suggestive of dislocation generation at the site of substrate imperfections.

Additionally, stacking faults and twins are not present in the Figure 2 micrograph. For conventional Si epitaxy, these types of defects have been shown to result from substrate contamination.[6,7] Their

absence in the present sample can probably be attributed to the excellent substrate cleanliness achieved by the UHV sputter-anneal technique.

An interesting comparison can be made between the SPE growth process and the recrystallization of amorphous Si layers created by high-dose ion implantation.[8] The similarity in the growth rates of these two processes suggests that the mechanisms which determine the kinetics of epitaxial crystallization are the same in both cases. In the vicinity of the substrate/film interface, an ion implanted sample and a deposited film may not differ significantly in physical structure. Ion implantation creates an extended region (typically several hundred Angstroms wide) over which the crystalline-to-amorphous transition occurs; deposited films may also contain such a transition layer. Jona has shown that extremely thin Si films (~15 Å) deposited on atomically clean, ordered Si surfaces exhibit crystalline order even when the substrates are held at room temperature during deposition.[9] Extending this finding to the case of thicker films such as those used in our work suggests that a region of intermediate crystallinity could exist near the substrate, but it would be covered eventually by a totally amorphous film. Sufficient data does not exist to permit estimating the thickness of this "transition layer," but work in this area is in progress.

In summary, we have demonstrated the growth of Si epitaxial layers of good crystallographic quality by the process of metal-free SPE. The combination of low-temperature growth, implicit thickness control, and compositional purity possible with this growth method should offer a unique capability for the fabrication of solid-state devices requiring extremely thin electrically active layers and/or sharp interfacial

doping profiles. Further investigations of the SPE growth process and of the electrical properties of layers grown by this technique are in progress.

The authors gratefully acknowledge the contributions of Wen Tseng of the California Institute of Technology, who performed the TEM analysis, and of S.S. Lau, who performed the channeling effect measurements and participated in many helpful discussions.

REFERENCES

1. B.A. Joyce, Rep. Prog. Phys. 37, 363 (1974).

2. C. Canali, J.W. Mayer, G. Ottaviani, D. Sigurd, and W.F. van der Weg, Appl. Phys. Lett. 25, 3 (1974).

3. C. Canali, S.U. Campisano, S.S. Lau, Z.L. Liau and J.W. Mayer, J. Appl. Phys. 46, 2831 (1975).

4. R.L. Boatright and J.O. McCaldin, J. Appl. Phys. 47, 2260 (1976).

5. A. Christou, J.E. Davey, H.M. Day, and H.B. Dietrich, Appl. Phys. Lett. 30, 598 (1977).

6. R.C. Henderson and R.F. Helm, Surf. Sci. 30, 310 (1972).

7. R.N. Thomas and M.H. Francombe, Surf. Sci. 25, 357 (1971).

8. L. Csepregi, J.W. Mayer, and T.W. Sigmon, Phys. Lett. 54A, 157 (1975).

9. F. Jona, Surfaces and Interfaces, Proc. 13th Sagamore Army Mat. Res. Conf., eds., J.J. Burke, N.C. Reed, and V. Weiss (Syracuse Univ. Press, New York, 1967).

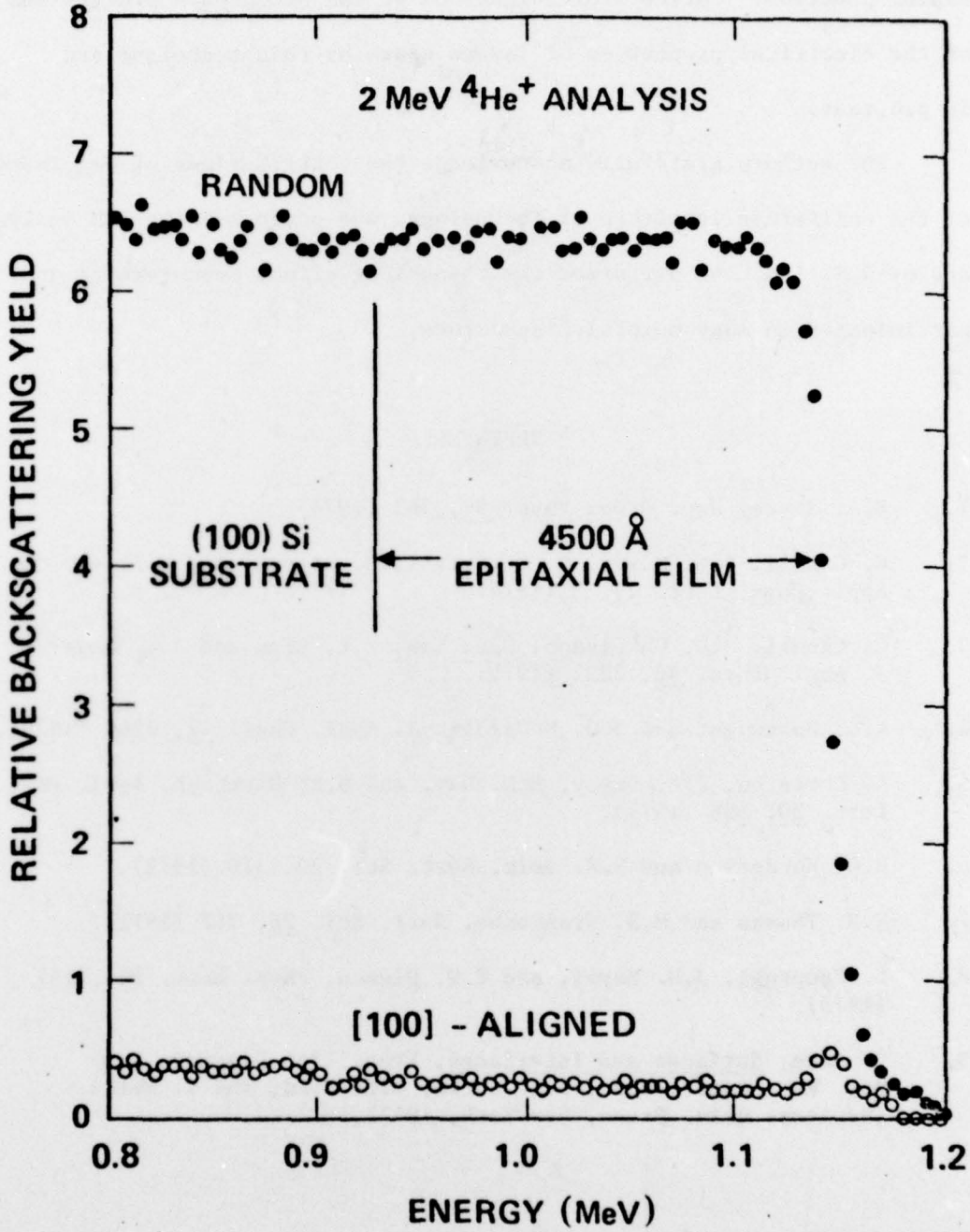

Figure 1. 2 MeV $^4He^+$ channeling spectra of an epitaxial Si layer grown by solid-phase epitaxy at 525 ± 25°C for 2 hr. [100]-aligned (channeled) data are shown by open circles, the non-channeled (random) yield by solid dots.

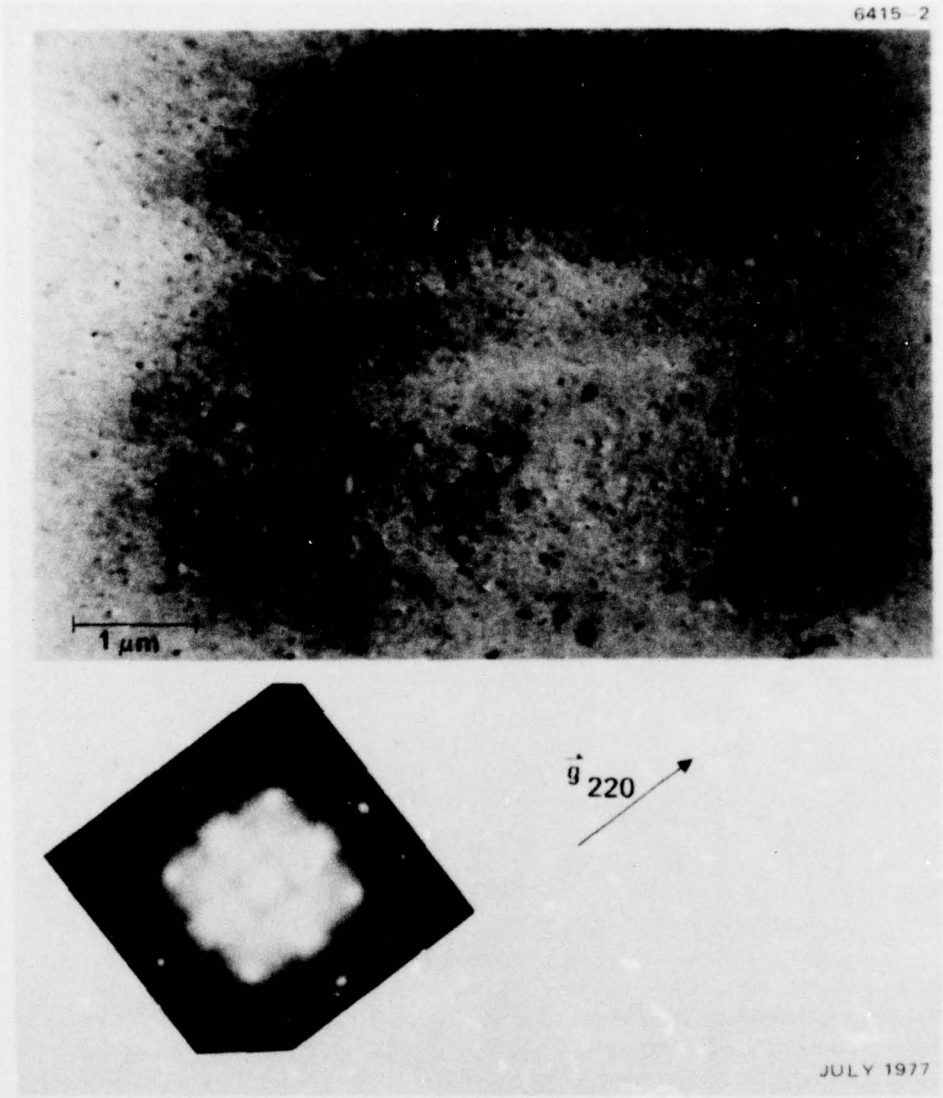

Figure 2. Bright-field transmission electron micrograph of a 4500 Å (100) Si film grown by solid-phase epitaxy at 525°C. Also shown is the corresponding selected-area diffraction pattern.